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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/827,389	04/19/2004	Chung-Cheng Chou	N1085-00209	3133

8933 7590 10/20/2006

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PHILADELPHIA, PA 19103-4196

EXAMINER

PHAM, LONG

ART UNIT PAPER NUMBER

2814

DATE MAILED: 10/20/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

**Office Action Summary**

Application No.

10/827,389

Applicant(s)

CHOU, CHUNG-CHENG

Examiner

Long Pham

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 24 July 2006.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1, 2, 4, 5 and 7-15 is/are pending in the application.
- 4a) Of the above claim(s) 8 and 13 is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1, 2, 4-5, 7, 9-12, and 14 and 15 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO/SB/08)  
Paper No(s)/Mail Date \_\_\_\_\_.
- 4) ☐ Interview Summary (PTO-413)  
Paper No(s)/Mail Date. \_\_\_\_\_.
- 5) ☐ Notice of Informal Patent Application
- 6) ☐ Other: \_\_\_\_\_.

## DETAILED ACTION

### Rejections and/or objections necessitated by the amendments

#### *Claim Rejections - 35 USC § 103*

The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

Claims 1-2, 4-5, 7, 9-12, 14, and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over the applicant's admitted prior art (AAPA) of this application in combination with Afgabi et al. (US publication 2003/0095427) and Lawlor (US pub 2004/0043587).

With respect to claims 1, 2, 7, 12, AAPA teaches a single transistor random access memory cell, comprising (see fig. 1 and the Field of the Invention):

A transfer gate 120; and

A storage capacitor with a storage node 150.

AAPA fails to teach that the storage node has an MOS native device.

Afgabi et al. teach a storage node having an MOS native device to reduce the charge leakage. See [0004] and [0005].

It would have been obvious to one of ordinary skill in the art of making semiconductor devices to incorporate the above teaching of Afgabi et al. into the device of AAPA to achieve the above benefit.

Further with respect to claims 1, 2, 7, and 12, since AAPA in combination with AAPA teach the claimed structure, an inversion layer having a near zero threshold voltage would inherently be formed under beneath the transfer gate.

Further with respect to claims 1, 2, 7, and 12, how the inversion layer is formed has not been given patentable weight since claims are directed to a device.

Further with respect to claim 1, AAPA further teaches a shallow trench isolation, STI, insulator 110 having a step height below that of a sidewall of a substrate insulator (the insulator between the capacitor plate 130 and substrate

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100 and the capacitor plate 130 covering the STI insulator and the sidewall. See fig. 1 and associated text of AAPA.

AAPA fails to teach that at least the sidewall of the substrate insulator is doped.

Lawlor teaches doping an insulator to increase its conductivity. See claim 11.

It would have been obvious to one of ordinary skill in the art of making semiconductor devices to incorporate the above teaching of Lawlor into the device of AAPA to achieve the above benefit.

With respect to claims 4, 9, and 14, AAPA further teaches that the transfer gate 120 and a capacitor plate 130 is being closer together than a minimum line width of a layer.

With respect to claims 5, 10, and 15, AAPA further teach a air spacer between the transfer 120 and capacitor plate 130 but fails to tech the spacer is made of dielectric.

However, the use of dielectric as insulating spacer or spacing is well-known.

Further with respect to claim 11, AAPA further teaches a shallow trench isolation, STI, insulator 110 having a step height below that of a sidewall of an insulator between the capacitor plate and substrate. See fig. 1 and associated text of this application.

Further with respect to claim 11, AAPA further teaches the transfer gate 120 and the capacitor are being in an active area of the substrate. See fig. 1 and associated text of this application.

Further with respect to claim 11, AAPA fails to teach an external MOS native device.

Afgabi et al. teach including an MOS native device to reduce the charge leakage. See [0004] and [0005].

Further with respect to claim 11, AAPA in combination Afgabi et al. further teach the capacitor plate covering the STI insulator and the external MOS native device.

It would have been obvious to one of ordinary skill in the art of making semiconductor devices to include an MOS native device in the device of Afbabi et al. to achieve the above benefit.

Further with respect to claim 11, AAPA in combination with Afgabi et al. further teach that the capacitor plate covering the STI insulator 110 and plate would inherently cover the MOS native device if incorporated into the device of AAPA.

### ***Response to Arguments***

Applicant's arguments with respect to claims 1-2, 4-5, 7, 9-12, 14, and 15 have been considered but are moot in view of the new ground(s) of rejection.

### ***Conclusion***

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

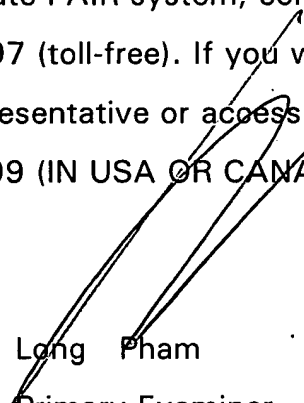
A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within **TWO MONTHS** of the mailing date of this final action and the advisory action is not mailed until after the end of the **THREE-MONTH** shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than **SIX MONTHS** from the date of this final action.

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Any inquiry concerning this communication or earlier communications from the examiner should be directed to Long Pham whose telephone number is 571-272-1714. The examiner can normally be reached on Mon-Frid, 10am to 5pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael Fahmy can be reached on 571-272-1705. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.



Long Pham  
Primary Examiner  
Art Unit 2814

LP